www-isl.stanford.edu/~abbas/group/papers_and_pub/cicc_98.pdf
(6/21/01)
↳ last modified

A Nyquist Rate Pixel Level ADC for CMOS Image Sensors

David X.D. Yang Boyd Fowler Abbas El Gamal

Information Systems Laboratory, Stanford University, Stanford, CA 94305-4055

Abstract

A Nyquist rate Multi-Channel Bit Serial (MCBS) ADC using successive comparisons is presented. The ADC is suited to pixel level implementation in a CMOS image sensor. It comprises a 1-bit comparator/latch pair per 4 pixels and a DAC/controller shared by all pixels. A CMOS 320 × 240 sensor using the MCBS ADC is described. It achieves 8.9×8.9 μm pixel size at 25% fill factor in 0.35 μm CMOS technology. Measured INL/DNL for the ADC are 2.3/1.2 LSB at 8-bit. Gain/offset FPN due to ADC are 0.24%/0.2%.

Introduction

CMOS technology holds out the promise of a single-chip digital camera. The simple approach of combining an analog CMOS sensor array, a high speed ADC followed by a digital signal processor on a single chip, although significantly reduces system cost and power, does not fully exploit the potential of integration and technology scaling. Integration provides the opportunity to rethink the basic partitioning of functionality among the pixel, column, and chip levels.

In this paper we focus on ADC implementation. ADC can be performed at the chip level using a high speed converter, at the column level using multiple lower speed converters, or at the pixel level using very simple low speed converters. Analysis by several authors [1, 2] shows that pixel level ADC should achieve the highest SNR and the lowest power consumption, since it is performed in parallel, close to where the signals are generated, and operates at very low speed. Unfortunately, none of the well established ADC techniques meets the stringent area and power requirements for a pixel level implementation. As a result most published work on ADC for image sensors is focused on column and chip level implementations, e.g. [2].

Few authors took up the challenge of implementing pixel-level ADC [3, 4, 5, 6, 7]. In [3, 4, 5] a voltage-to-frequency (VF) converter is used at each pixel so that no analog signals need to be transported. However, since the ADC is performed one row at a time, this method is essentially a column ADC method rather than a true fully parallel pixel level ADC. In [6, 7] the first true pixel level ADC technique is described. The ADC employs a one bit $\Sigma\Delta$ modulator at each pixel. The ADCs are implemented using very simple and robust circuits, and operate in parallel. However, the implementation has several shortcomings including: large pixel size, high output data due to oversampling, poor low light performance and high fixed pattern noise. The large pixel size problem quickly disappears with technology scaling as we demonstrate in this paper. In fact, if photodetectors are to be built on top of a CMOS chip, pixel level ADC may require no additional area.

In this paper, we introduce the first viable Nyquist-rate pixel level ADC technique. The technique, which we denote by Multi-Channel Bit Serial (MCBS) ADC uses successive comparisons to output one bit at a time simultaneously from all pixels. It can still be implemented using simple robust circuits and overcomes the shortcomings of our $\Sigma\Delta$ ADC. Output data rate is reduced by using Nyquist rate conversion instead of oversampling. Low light performance is improved to the level of analog CMOS sensors by using direct integration instead of continuous sampling. Nonuniformity is significantly reduced by globally distributing the signals needed to operate the ADC and by performing local autozeroing. The method has an additional important advantage; the ADCs can be fully tested by applying electrical signals externally instead of light.

The remainder of this paper is organized as follows. In the next section we describe the operation of the MCBS ADC. In the following section we discuss pixel circuit design and layout. Finally we present measured results from a 320×240 image sensor with MCBS ADC.

MCBS ADC Operation

The severe constraints on pixel area and fill factor preclude the use of existing ADC techniques. Traditional bit-parallel techniques such as single slope require an m-bit latch at each pixel to implement m-bit conversion, which is not feasible for typical m values. Moreover, bit-serial techniques such as successive approximation or algorithmic ADC require complex circuits with very precise

and matched analog components. As a result, they are also not suited to pixel level implementation.

Before we describe the operation of our MCBS ADC we make the following crucial observation. Note that an ADC maps an analog signal S into a digital representation (codeword) according to a quantization table. A 3-bit Gray coded example is given in Table 1, where S is assumed to take values in the unit interval (0,1]. The table lists the assignment of each input range to a 3-bit codeword. The crucial observation is that we can generate each bit of the codeword independently. For example consider the generation of the LSB. From the table, the LSB is a 1 when $S \in (\frac{1}{8}, \frac{3}{8}] \cup (\frac{5}{8}, \frac{7}{8}]$ and a 0 otherwise. To generate the LSB, any bit-serial Nyquist-rate ADC must be able to answer the question: is $S \in (\frac{1}{8}, \frac{3}{8}] \cup (\frac{5}{8}, \frac{7}{8}]$?. Thus, the ADC is essentially a one-detector that indicates the input ranges resulting in a 1. Interestingly, this one-detector can be simply implemented using a one-bit comparator and a one-bit latch.

ADC Input Range	Codeword
$0 - \frac{1}{8}$	0 0 0
$\frac{1}{8} - \frac{2}{8}$	0 0 1
$\frac{2}{8} - \frac{3}{8}$	0 1 1
$\frac{3}{8} - \frac{4}{8}$	0 1 0
$\frac{4}{8} - \frac{5}{8}$	1 1 0
$\frac{5}{8} - \frac{6}{8}$	1 1 1
$\frac{6}{8} - \frac{7}{8}$	1 0 1
$\frac{7}{8} - 1$	1 0 0

Table 1: Codewords for m=3

A block diagram of the one-detector, which constitutes one channel of the MCBS ADC is shown in Figure 1. The analog signal S is connected to the positive terminal of the comparator, and the signal **RAMP**, which is an increasing staircase waveform, is connected to the negative terminal. The output of the comparator feeds into the gate of the latch, and the digital signal **BITX** connects to the data terminal of the latch. To generate the LSB, **RAMP** starts at zero and monotonically steps through the boundary points $(\frac{1}{8}, \frac{3}{8}, \frac{5}{8}, \frac{7}{8})$. At the same time, **BITX** starts at zero and changes *whenever* **RAMP** changes[1]. As soon as **RAMP** exceeds S, the comparator flips, causing the latch to store the **BITX** value just after the **RAMP** changes. The stored value is the desired LSB. After the comparator flips, **RAMP** continues on, but since **RAMP** is monotonic, the comparator flips exactly once so that the latch keeps the desired value. As shown in Figure 1, for input1, the comparator flips when **RAMP** steps to $\frac{5}{8}$, latching **BITX**, which is 0, and for input2 a 1 is latched. After **RAMP** completes stepping through the boundary points, the latched output is read out. Then **RAMP** and **BITX** are reset to zero in preparation for another sequence of comparisons. The MSB is similarly generated by comparing S to $\frac{4}{8}$ and the NMSB is generated by comparing S to $\frac{2}{8}$ and to $\frac{6}{8}$.

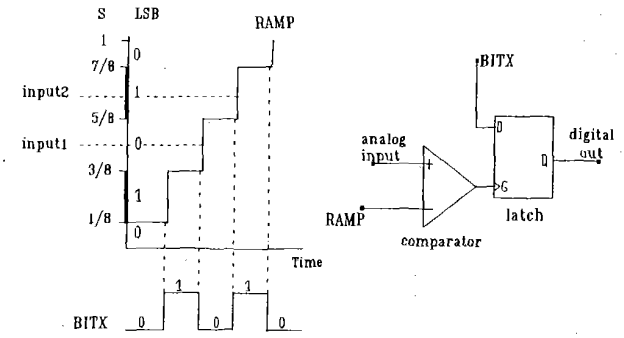

Figure 1: One-detector operation.

This 3-bit example can be easily generalized to perform any m-bit ADC. To quantize S to m bits of precision, the unit interval is divided into 2^m input ranges $(\frac{i}{2^m}, \frac{(i+1)}{2^m}]$, $0 \leq i \leq 2^m - 1$, and each range is represented by an m-bit codeword. To determine the m-bit codeword for S, the ADC generates each bit serially (in any desired order). Each bit is generated by answering the question: is signal $S \in A$?, where A is the set of input ranges that result in 1. The ADC implements the question by successive comparisons at the boundary points of the ranges in A using the one-detector described. The **RAMP** signal steps through the boundary values monotonically, while **BITX** indicates the value (0 or 1) of the particular range. At the end of each sequence of comparisons, the latched value is read out.

The number of comparisons performed for each bit varies, e.g. in the 3-bit example, generating the LSB requires 4 comparisons, the NMSB 2 comparisons and the MSB only 1 comparison. It can be shown that for m-bits of precision, a total of at least $2^m - 1$ comparisons are needed for any code, and that the Gray code achieves this lower bound. Thus in addition to being robust against single errors, the Gray code also minimizes the number of comparisons needed.

Although we assumed a uniform quantization table in our discussion, it is easy to see that our ADC can implement any quantization table, e.g. ranges corresponding to logarithmic or gamma correction functions[2].

A block diagram of the MCBS ADC is shown in Figure 2. It comprises a one-detector at each pixel or shared

[1]To meet the setup time requirement of the latch, **BITX** must transition slightly before **RAMP** changes.

[2]In this case the **RAMP** signal should have higher precision than m.

among a group of neighboring pixels. The **RAMP** and **BITX** are globally distributed. The shared circuits consist of a simple state-machine and an m-bit DAC. The state-machine produces **BITX** and the input to the DAC necessary to generate the **RAMP** signal.

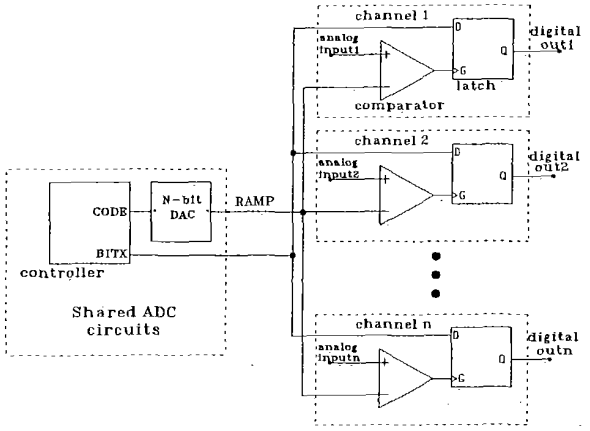

Figure 2: MCBS ADC Block Diagram.

Pixel Circuit Design

A schematic of four pixels sharing a one-detector circuit is shown in Figure 3. The circuit uses 18 transistors. The comparator consists of a transconductance amplifier followed by a Wilson current mirror and a cascode output load. It is biased to operate in subthreshold to maximize gain and minimize power. The latch operates as a 2T DRAM cell where M1 is the write port pass transistor and M2 is the read port buffer. Pixel nonuniformity is reduced by sharing the circuits that generate the global signals, which constitute the most complex ADC circuits. The nonuniformity due to the one-detector circuit arises from two sources: variation in analog switching feedthrough and comparator offset. Comparator offset is reduced by autozeroing, which is accomplished by storing the offset value on the photodiode capacitor by briefly turning on M4 after conversion is completed.

The layout of a 2×2 pixel block is shown in Figure 4. The layout is symmetrically organized to reduce fixed pattern noise among the four pixels and to ensure uniform spatial sampling. This includes using identical geometry photodiodes with equal spacings among them, implementing capacitor M5 using four symmetrically placed MOS transistors, and ensuring that the photodiodes have very similar wire and transistor surroundings. The effect of pixel circuit induced substrate noise, e.g. impact ionization noise, on the $n^+ - p_{sub}$ photodiodes is minimized by using PMOS transistors (in an

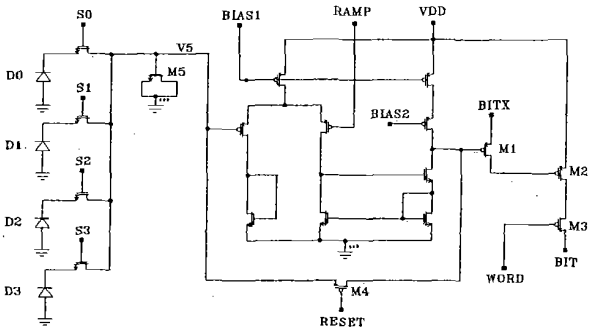

Figure 3: Four pixels sharing a one-detector circuit.

nwell) whenever possible. Since a salicide block mask was not available, we attempted to improve quantum efficiency using field oxide cuts in the n^+ diffusion, and hence the spiral-shaped photodiodes. To prevent light induced currents from affecting the analog circuitry or causing latchup, we used metal4 as a light shield everywhere except over the photodetectors.

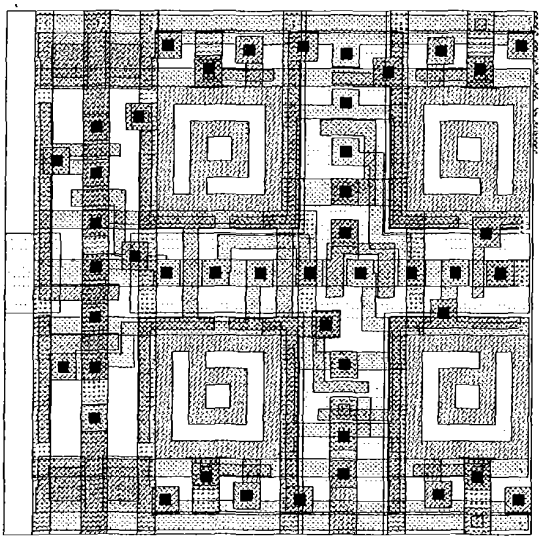

Figure 4: Layout of a 2×2 pixel block.

A 320x240 Image Sensor

A 320 × 240 image sensor with the MCBS ADC was designed and fabricated in a 0.35μm CMOS process. The chip consists of a 160×120 array of 2×2 pixel blocks, each sharing the one-detector circuit described, a row decoder, column sense amplifiers and multiplexers. The sensor architecture and image readout is very similar to a ROM, as described in [7]. The main characteristics of the chip

are listed in Table 2. Since each one-detector is multiplexed among four pixels, the sensor outputs one quarter frame at a time. Each quarter frame is read out one bit plane at a time.

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor Area	3027 μm × 2328 μm
Pixel Area	8.9 μm × 8.9 μm
Transistors per pixel	4.5 (18 per four pixels)
Fill Factor	25%
Package	224 pin PGA
Supply Voltage	3.3 v

Table 2: 320×240 Area Image Sensor Characteristics

An important advantage of the MCBS ADC is that it is electrically testable. To test the ADC the photodetectors are disconnected by turning off all select transistors. The one-detector input (node v5 in Figure 3) is then set to the desired **RAMP** value by turning on M4, and the its output is read out. The ADC transfer function can be determined by sweeping the input voltage range. Figure 5 shows the measured ADC transfer functions for 16 pixel blocks. The ADC measured integral and differential nonlinearites are 2.3 LSB and 1.2 LSB at 8 bits, respectively. The pixel gain and offset FPN due to ADC are 0.24% and 0.2% respectively.

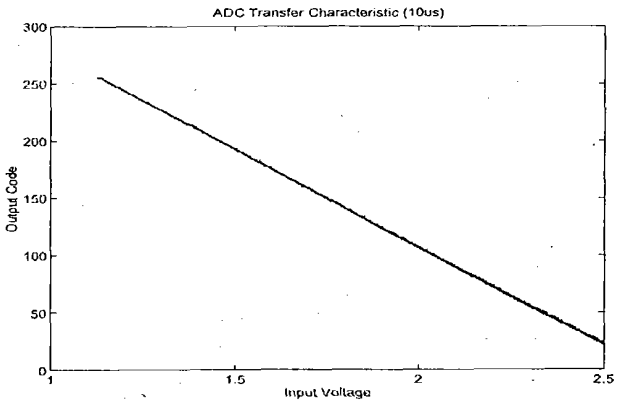

Figure 5: ADC transfer curve at 10 μs conversion time.

A sample image caputured by the sensor is shown in Figure 6. We were not able to capture a higher quality image as a result of the high MOS transistor leakage due to drain induced barrier lowering (DIBL), substrate noise due to digital output buffer switching, and the very low quantum efficiency due to salicide.

Conclusion

We have introduced the first viable Nyquist rate pixel level ADC technique. The ADC requires very simple and robust circuits, which can be implemented in a standard CMOS process. We demonstrated experimentally that the ADC achieves a high enough level of performance for image sensor applications. The ADC results in very low FPN and can be fully tested electrically. We believe that this ADC technique goes a long ways towards realizing the potential of pixel level ADC.

Acknowledgments

We would like to acknowledge the generous support of Intel Corp. and the Hewlett Packard Co. and the contributions of M. Hao, X. Liu and M. Godfrey to the design and testing of the sensor.

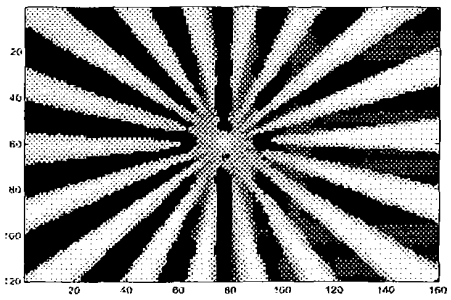

Figure 6: A 160x120 image

References

[1] U. Ringh, C. Jansson, and K. Liddiard. Readout concept employing a novel on Chip 16 bit ADC for smart IR focal plane arrays. *Proceedings of SPIE*, Vol. 2745, 1996.

[2] B. Pain and E. Fossum. Approaches and analysis for on-focal-plane analog-to-digital conversion. *Proceedings of SPIE*, vol. 2226, 1994.

[3] B. Pain, S. Mendis, R. Schober, R. Nixon, and E. Fossum. Low-power low-noise analog circuits for on-focal-plane signal processing of infrared sensors. *Proceedings of SPIE*, Vol. 1946, 1993.

[4] U. Ringh, C. Jansson, C. Svensson, and K. Liddiard. CMOS analog to digital conversion for uncooled bolometer infrared detector arrays. *Proceedings of SPIE*, Vol. 2474, 1995.

[5] W. Yang. A Wide-Dynamic-Range, Low-Power Photosensor Array. *ISSCC Digest of Technical Papers*, San Fransico, CA, February 1994.

[6] B. Fowler, A. El Gamal, and D. X. D. Yang. A CMOS Area Image Sensor with Pixel-Level A/D Conversion. *ISSCC Digest of Technical Papers*, San Fransico, CA, February 1994.

[7] D. Yang, B. Fowler, and A. El Gamal. A 128×128 Pixel CMOS Area Image Sensor with Multiplexed Pixel Level A/D Conversion . *IEEE 1996 Custom Integrated Circuits Conference*, San Diego, CA, May 1996.